

SRI VASAVI INSTITUTE OF ENGINEERING & TECHNOLOGY

An Autonomous Institute

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK Kakinada)
Accredited by NBA (Mech, ECE, CSE) & NAAC, An ISO 9001:2015 Certified Institute
Nandamuru, Pedana Mandal, Krishna Dist – 521369.



Date : 11-01-2024

MTECH I SEMESTER (R19 REGULATION) II MID EXAMINATIONS, JANUARY - 2024

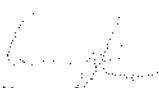
TIME TABLE

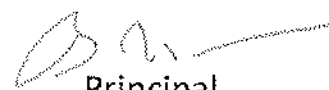
TIME : 10.00 AM TO 12.00 AM

DEPARTMENT	22-01-2024 (MONDAY)	23-01-2024 (TUESDAY)	24-01-2024 (WEDNESDAY)	25-01-2024 (THURSDAY)	27-01-2024 (SATURDAY)
ECE (VLSI System Design - 61)	CMOS ANALOG IC DESIGN (M23EC11) <i>GN</i>	CMOS DIGITAL IC DESIGN (M23EC12) <i>MRA</i>	Elective – I VLSI TECHNOLOGY (M23EC13A) <i>YRR</i>	Elective – II DEVICE MODELING (M23EC14A)	RESEARCH METHODOLOGY AND IPR (M23EC15)

NOTE:

- Any Omissions or clashes in this time table may please be informed to the controller of examination immediately.
- The HOD's are requested to inform the Controller of Examination any other substitute subjects that are not included in the above time table immediately.


Controller of Examinations


Principal

Copy to:

- Chairman, Secretary, Correspondent,
- Executive Directors,
- Controller of Examination,
- Hod's – ECE & CSE,
- Main Notice Board, Student's Notice Board, Circular file & Exam Cell