SRI VASAVI [illegible]STITUTE OF ENGINEERING [illegible] TECHNOLOGY

An Autonomous Institute

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK Kakinada)

Accredited by NBA (Mech, ECE, CSE) & NAAC, An ISO 9001:2015 Certified Institute

Nandamuru, Pedana Mandal, Krishna Dist – 521369.

Date : 11-01-2024

M.TECH I SEMESTER (R19 REGULATION) II MID EXAMINATIONS, JANUARY - 2024

TIME TABLE

TIME : 10.00 AM TO 12.00 AM

[illegible]	22-01-2024 (MONDAY)	23-01-2024 (TUESDAY)	24-01-2024 (WEDNESDAY)	25-01-2024 (THURSDAY)	27-01-2024 (SATURDAY)
ECE (VLSI System Design - 61)	CMOS ANALOG IC DESIGN (M23EC11)	CMOS DIGITAL IC DESIGN (M23EC12)	Elective – I VLSI TECHNOLOGY (M23EC13A)	Elective – II DEVICE MODELING (M23EC14A)	RESEARCH METHODOLOGY AND IPR (M23EC15)

NOTE:

i. Any Omissions or clashes in this time table may please be informed to the controller of examination immediately.

ii. The HOD's are requested to inform the Controller of Examination any other substitute subjects that are not included in the above time table immediately.

Controller of Examinations

Principal

Copy to:

1) Chairman, Secretary, Correspondent,
2) Executive Directors,
3) Controller of Examination,
4) Hod's – ECE & CSE,
5) Main Notice Board, Student's Notice Board, Circular file & Exam Cell