

## **Quality of internal semester Question papers, Assignments and Evaluation (20)**

*(Mention the initiatives, implementation details and analysis of learning levels related to quality of semester question papers, assignments and evaluation)*

### **Internal Assessment Test:**

The institute conducts two internal assessment tests after completing 8<sup>th</sup> week and 16<sup>th</sup> week respectively. Each test covers half of the syllabus. The tests are conducted for a maximum of 30 marks. (No minimum marks criteria from the university). The duration of the test is one and half hour and question paper is set to make the student to learn time management. Program Coordinator along with test coordinator is responsible for the conduction of the test. The department has a Scrutinizing Committee, comprising of HoD and two senior faculty members to check the quality of the question paper, RBT levels and COs compliance.

### **Process for Internal Assessment Test Question Paper Setting:**

- The course co-coordinator sets the question paper for the Internal Assessment.
- The course co-coordinator ensures to frame questions based on various RBT levels and is mapped to the Course Outcomes (COs) to assess the students at various RBT levels.

### **Procedure for Conduction and Evaluation of Internal Assessment Test:**

The time table for the Internal Assessment Test will be conducted as per academic calendar and the dates are announced and kept in the notice board 15 days prior to the commencement of the test.


### **Question Papers:**

For each subjects, question bank is prepared. While setting the question paper all previous university exam papers are taken into consideration. According to level of toughness the questions are prepared (viz., analyzing the problems, implementation of modern tools, formulating the problems etc), which is termed as Bloom's Taxonomy.

The questions will be of three categories:

- One third of the questions is straight and can be answered by all students.
- One third of the questions need analysis and use of content covered as per syllabus.
- Remaining one third of the questions are not straight. Certain amount of thinking, analysis and mathematical knowledge are required to resolve.

A question paper template is shown in the following figure

ACADEMIC YEAR	Hall Ticket No:
 <b>SRI VASAVI</b> INSTITUTE OF ENGINEERING & TECHNOLOGY NANDAMURU, PEDANA. 521 369.	
III B.Tech. I SEM I Mid Examinations	Subject:
Branch:	Time:
Max.Marks:30	Date:
Don't Write Anything on question paper	

**Assignments:**

- Assignment issue and submission dates are announced by the respective faculty members. Assignment questions are prepared using Bloom's Taxonomy process.
- Surprise tests, quizzes, video links are provided.
- In order to bridge the gap in curriculum, bright students are given some assignment beyond syllabus.
- Assignments are evaluated and feedback is given to the students to improve their learning and appreciate their efforts

**Evaluation:**

The faculties after every internal assessment test, they explain the solution of the questions in the class which will enable them to perform well in the final examination.

For any genuine reasons, if a student was unable to perform well in the given two internal assessment tests, improvement test is given to him/her.

For R-16 regulation, 80% of the marks are considered from one of the internal and 20% of the marks are considered from the other internal exam and for R-13 regulation out of two internal exams one best internal is considered. If a candidate remains absent for all the tests conducted, the Internal assessment marks are marked as “Absent” in the result. Assignments are used as a tool for practice and evaluation is based purely on Internal Assessment Test

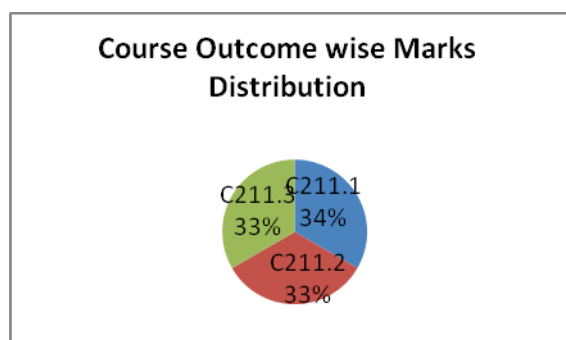
### Sample Internal Question Paper Analysis:

**Name of the Course: Electronic Devices and Circuits**  
**Sem Course Code: C211**

**Year & Semester: II Year I**  
**INTERNAL: 1**

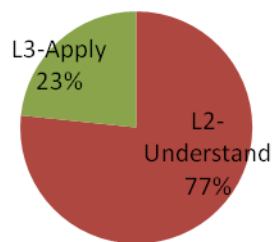
Q.No	Question	Marks	CO	TL
1.a	Describe the Hall Effect. What properties of a semiconductor are determined from a Hall Effect experiment?	5	C211.1	Understand
1.b	In an N type semiconductor the fermi level is 0.3 ev below the conduction band at 300k. If the temperature is increased to 360 k, If the temperature is increased to 360 k, determine the new position of Fermi level.	5	C211.1	Apply
2.a	Explain the operations of Tunnel diode with the help of Energy band diagrams.	8	C211.2	Understand
2.b	The reverse saturation current of Ge diode is 2 micro amps at a temperature of 25 degree centigrade. Find the reverse saturation current of the diode at a temperature of 75 degree centigrade.	2	C211.2	Apply
3.a	Explain the operation of Bridge Rectifier and derive its ripple factor.	5	C211.3	Understand
3.b	Explain the operation of Full Wave Rectifier with shunt Capacitor filter and derive its ripple factor.	5	C211.3	Understand

CO	Marks	%
C211.1	10	33.33
C211.2	10	33.33
C211.3	10	33.33



TL	Marks	%
L1-Remember		
L2-Understand	23	76.67
L3-Apply	7	23.33
L4-Analyze		
L5-Evaluate		
L6-Create		

**Bloom's Level wise Marks Distribution**



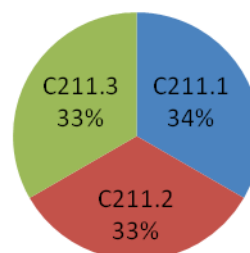
Name of the Course: Electronic Devices and Circuits  
Sem Course Code: C211

Year & Semester: II Year I  
INTERNAL: 2

Q.No	Question	Marks	CO	TL
1.a	How BJT acts as an Amplifier	5	C211.4	Understand
1.b	Explain the construction and operation of Enhancement MOSFET.	5	C211.4	Understand
2	Define Stability Factor and derive the Stability Factor for Self Bias circuit.	10	C211.5	Apply
3	Draw the neat circuit diagram of CE amplifier in terms of h parameters. Determine Current gain, input resistance, voltage gain and output admittance using exact analysis.	10	C211.6	Understand

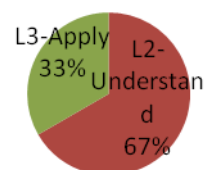
CO	Marks	%
C211.1	10	33.33
C211.2	10	33.33
C211.3	10	33.33

**Course Outcome wise Marks Distribution**



TL	Marks	%
L1-Remember		
L2-Understand	20	66.67
L3-Apply	10	33.33
L4-Analyze		
L5-Evaluate		
L6-Create		

**Bloom's Level wise Marks Distribution**



## Evaluation Quality:

Each faculty prepares scheme of evaluation and also the key for each exam conducted to students. The answer sheets after evaluation will be distributed to students in the class room and discuss the answers with students. If there are any grivances, same will be discussed and resolved.

A Sample Scheme of Evaluation for EDC Internal Question Paper is shown below:

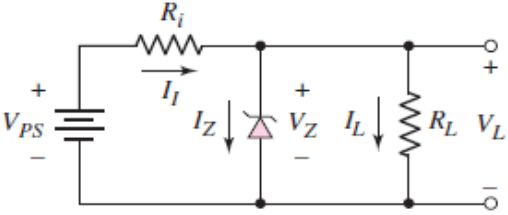
<b>Department of Electronics &amp; Communication Engineering</b>	
II B.Tech-I Sem I Mid Exam	SUB:EDC
Branch:ECE A&B	MAX Marks :30M
A.Y -2017-2018	
<b><u>Scheme of Evaluation</u></b>	
1. 1.a) A) Describe the Hall Effect.	(2M)
What properties of a semiconductor are determined from a Hall Effect experiment?	(3M)
B) In an N type semiconductor, the Fermi level is 0.3 ev below the conduction band at 300 k. If the temperature is increased to 360 K, determine the new position of Fermi level.	(5M)
2. A) Explain the operation of Tunnel diode with the help of Energy band diagrams.	(8M)
B) The reverse saturation current of Ge diode is 2 micro amps at a temperature of 25 degree centigrade. Find the reverse saturation current of the diode at a temperature of 75 degree centigrade.	(2M)
3. A) Explain the operation of Bridge Rectifier.	(2M)
Derive its ripple factor.	(3M)
B ) Explain the operation of Full Wave Rectifier with shunt Capacitor filter.	(2M)
Derive its ripple factor.	(3M)
Total: 30 Marks	

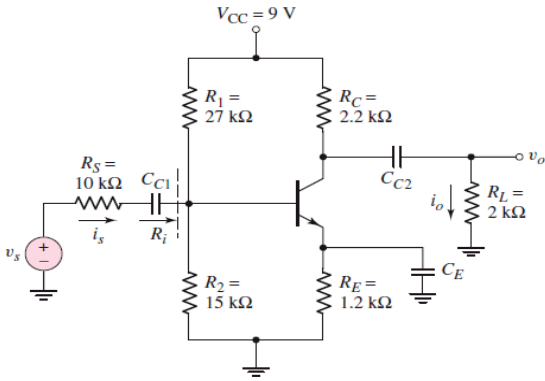
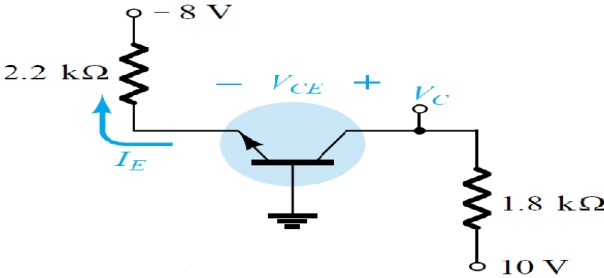
## Sample Assignment Question Paper Analysis:

Name of the Course: Electronic Devices and Circuits  
Sem Course Code: C211

Year & Semester: II Year I  
Assignment Questions

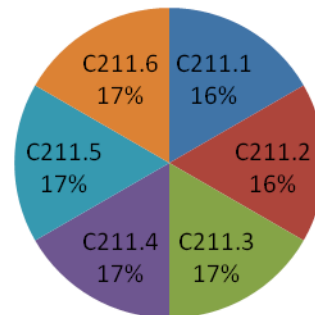
Q NO	Assessment question	Marks	Connected CO	BTL of CO
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A1.1	Consider silicon at $T = 300$ K doped with phosphorus at a concentration of $N_d = 10^{16} \text{ cm}^{-3}$ . $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ . Calculate electron & hole concentrations in this semiconductor.	2M	C211.1	Apply
A1.2	Define Hall Effect and Derive Hall coefficient expression along with applications of Hall Effect.	1M		Apply
A1.3	Derive continuity equation and state its special cases.	2M		Apply
A2.1	With minority carrier profile, derive expression for diode current in PN junction diode under forward bias condition.	2M	C211.2	Apply
A2.2	A diode is doped with $N_A = 10^{18} / \text{cm}^3$ on the p-type side and $N_D = 10^{15} / \text{cm}^3$ on the n-type side. Calculate the depletion-region width $w$ and built-in voltage? Assume $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$	2M		Apply
A2.3	Explain in detail about V-I characteristics of a Zener diode.	1M		Understand
A3.1	Design a voltage regulator using the circuit shown below. The voltage regulator is to power a car radio at $V_L = 9$ V from an automobile battery whose voltage may vary between 11 and 13.6 V. The current is $100 \text{ mA}$ . 	2M	C211.3	Create
A3.2	With circuit and necessary waveforms, explain the operation of Bridge Rectifier.	1M		Understand
A3.3	Derive an expression for ripple factor for FWR with capacitor filter.	2M		Apply
A4.1	With a neat sketch, explain the different current components of a transistor in forward active region.	2M	C211.4	Understand
A4.2	With the diagram of minority carrier profile, derive an expression for $\beta$ in NPN transistor in forward active region.	1M		Apply
A4.3	Draw and explain the drain characteristics of N-channel enhancement type.	2M		Understand
A5.1	Determine the stability factor for a CE amplifier by using self biased circuit.	1M	C211.5	Understand

A5.2	<p>For the circuit shown in Fig 1, determine (a) <math>I_B</math>, <math>I_C</math>, <math>V_{CE}</math>, <math>g_m</math> (b) <math>R_i</math>, <math>A_v</math>, <math>R_o</math>.</p>  <p style="text-align: center;">Fig 1</p>	2M		Analyze
A5.3	<p>For the circuit shown in Fig 3a, calculate <math>I_E</math>, <math>V_{CE}</math>, <math>V_C</math>. Assume <math>\beta=100</math>, <math>V_{BE}=0.7</math>.</p>  <p style="text-align: center;">Fig.2</p>	2M		Apply
A6.1	<p>A CE amplifier is drawn by a voltage source of internal resistance <math>R_s = 1000 \Omega</math>. The h-parameters are <math>h_{ie} = 1 \text{ K}\Omega</math>, <math>h_{re} = 2 \times 10^{-4}</math>, <math>h_{fe} = 50</math>, <math>h_{oe} = 25 \mu\text{A/V}</math>. Calculate the current gain, voltage gain and output resistance using exact analysis.</p>	2M	C211.6	Apply
A6.2	<p>Compare CE, CB, CC amplifiers</p>	1M		Understand
A6.3	<p>With neat circuit diagram, derive an expression for voltage gain in CS amplifier.</p>	2M		Understand

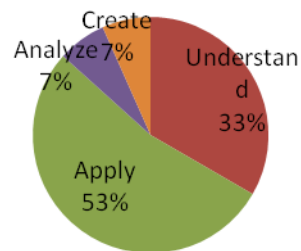
CO#	Marks	Percentage
C211.1	5	16.67
C211.2	5	16.67
C211.3	5	16.67
C211.4	5	16.67
C211.5	5	16.67
C211.6	5	16.67

### Course Outcome Wise Marks distribution Analysis in %



BTL	Marks	Percentage
Remember		
Understand	10	33.33
Apply	16	53.33
Analyze	2	6.67
Evaluate		
Create	2	6.67

### Blooms Level Marks distribution in %



#### Sample End Semester Paper Analysis:

Name of the Course: Electronic Devices and Circuits  
Sem Course Code: C211

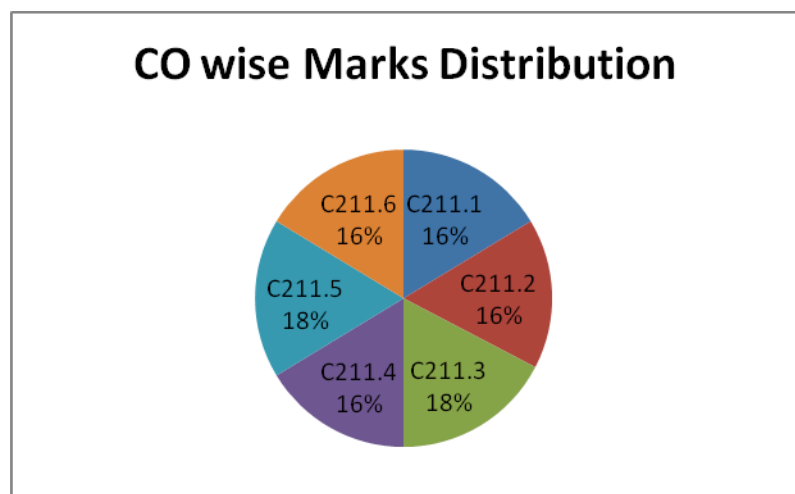
Year & Semester: II Year I  
Semester End Paper- SET 1

OCT/NOV-2017 University Q.Paper Analysis				SET-1
Q.No	Question	Marks	CO	TL
1.a	What is intrinsic semiconductor?	2	C211.1	remember
1.b	Write the disadvantages of LED	2	C211.2	remember
1.c	Define Ripple factor and peak inverse voltage	3	C211.3	remember
1.d	Write the applications of JFET	2	C211.4	remember
1.e	What are the advantages of self-biasing circuit?	3	C211.5	remember
1.f	What is emitter follower?	2	C211.6	remember
2.a	Explain in detail about Hall effect	7	C211.1	understand
2.b	Calculate the resistivity of intrinsic germanium at 300 <sup>0</sup> K. Assume $n_i = 2 \times 10^{13}$ per cm <sup>3</sup> , $\mu_n = 3800$ cm <sup>2</sup> /V - s and $\mu_p = 1800$ cm <sup>2</sup> /V - s	7	C211.1	apply
3.a	Explain the formation of depletion region in a PN junction	7	C211.2	understand

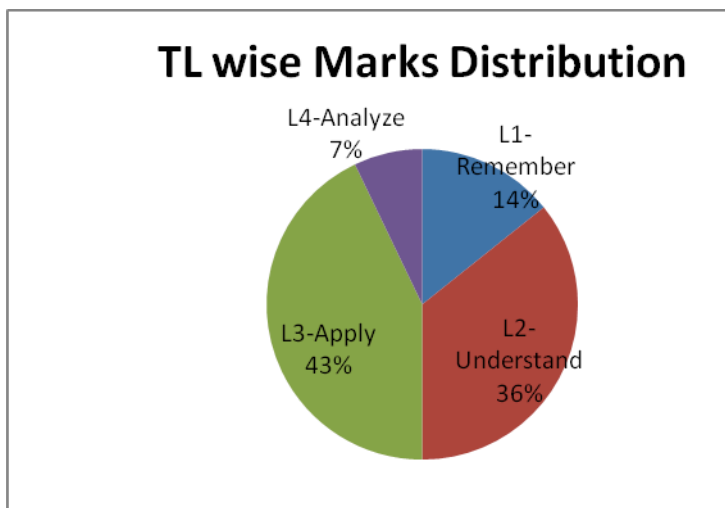


3.b	A P-N junction silicon diode has a reverse saturation current of 50nA at room temperature $27^{\circ}\text{K}$ . If the new reverse saturation current is observed to be 160nA , calculate the value of new temperature.	7	C211.2	apply
4.a	Draw and explain the circuit diagram of full wave rectifier with L-section filter	7	C211.3	understand
4.b	In half-wave rectifier an ac voltage of peak value 24V is connected in series with silicon diode and load resistance of $480\Omega$ . If the forward resistance of the diode is $20\Omega$ , find average load current and rms value of load current.	7	C211.3	apply
5.a	Explain input and output characteristics of a transistor in CB configuration	7	C211.4	understand
5.b	A certain JFET operates in the linear region with a constant drain voltage of 1V. When the gate voltage is 2V, a drain current of 10mA flows, but when gate voltage is changed to 1V, the drain current becomes 22.8mA. Find (a) the pinch-off voltage (b)the channel resistance for zero gate voltage	7	C211.4	apply
6.a	Explain any two bias compensation techniques	7	C211.5	understand
6.b	An npn transistor if $\beta = 50$ is used in CE circuit with $V_{CC} = 10\text{V}$ , $R_C = 2\text{K}\Omega$ . The bias is obtained by connecting $100\text{k}\Omega$ resistor from collector to base. Find the quiescent point and stability factor.	7	C211.5	apply
7.a	Draw the h-parameters equivalent circuit for a common emitter amplifier and derive the Expression for $A_i$ , $R_i$ , $A_v$ .	7	C211.6	apply
7.b	Compare the performance of BJT as an amplifier in CE, CB, CC configuration	7	C211.6	analyze

CO	Marks	%
C211.1	16	16.3265
C211.2	16	16.3265
C211.3	17	17.3469
C211.4	16	16.3265
C211.5	17	17.3469
C211.6	16	16.3265

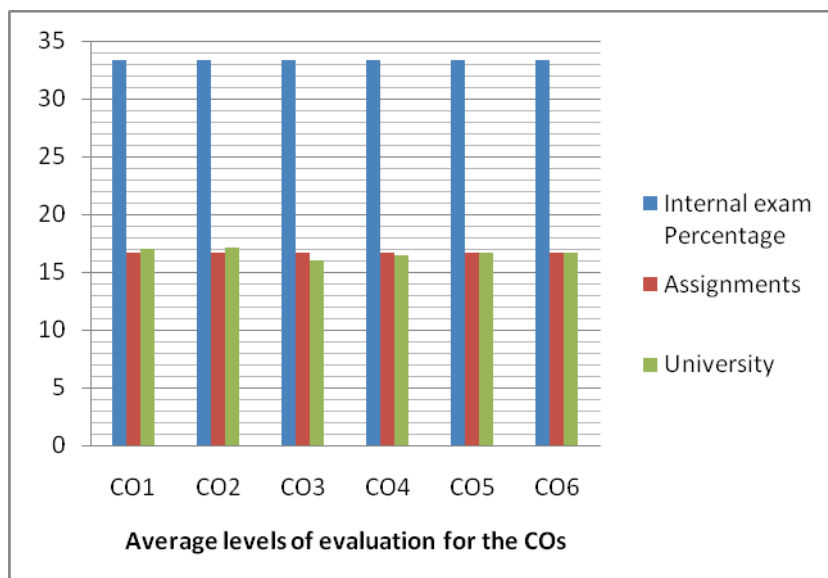


TL	Marks	%
L1-Remember	14	14.2857
L2-Understand	35	35.7142
L3-Apply	42	42.8571
L4-Analyze	7	7.14285
L5-Evaluate		
L6-Create		



#### Average levels of evaluation for the COs (2017-18):

COs	CO1	CO2	CO3	CO4	CO5	CO6
Internal exam Percentage	33.33	33.33	33.33	33.33	33.33	33.33
Assignments	16.67	16.67	16.67	16.67	16.67	16.67
University	16.99	17.15	16.05	16.40	16.63	16.66



#### Average levels of Taxonomy evaluation:

COs	Remember	Understand	Apply	Analyze	Evaluate	Create
Internal exam	9.60	39.23	15.34	8.98	4.47	4.44

Percentage						
Assignments	21.51	49.78	24.97	17.77	14	8.75
University	14.94	51.45	22.48	17.90	11.11	16.32

